

## Current Drive Circuit and Display

### Background of the Invention:

#### Field of the Invention:

5           The present invention relates to a current drive circuit and display, and more particularly to a current drive circuit of organic EL elements and display.

#### Description of the Related Art:

          Since the luminance of emitted light in an organic EL element is determined by the drive current, a current drive can better eliminate variation in  
10   the luminance of emitted light than a voltage drive in a display in which a plurality of organic EL elements is arranged in a matrix. Conventionally, a configuration such as shown in FIG. 1 is employed as the current drive circuit of organic EL elements. FIG. 1 is a circuit diagram of a current drive circuit of the prior art. As shown in FIG. 1, the current drive circuit of the prior art is provided  
15   with: p-channel MOS transistor M01, p-channel MOS transistor M11, reference current source I1, switch means SW1, and output terminal O1; organic EL element Z1 being connected to output terminal O1 as load. In addition, p-channel MOS transistor M01 and p-channel MOS transistor M11 constitute a current mirror circuit, whereby the current IREF that is generated by reference  
20   current source I1 is returned from high level power supply VDD and supplied by way of switch means SW1 to organic EL element Z1 that is connected to output terminal O1. Switch means SW1 is consisted of, for example, a p-channel MOS transistor and is ON/OFF controlled by one-bit graduation data signal D1. When switch means SW1 is turned ON, a prescribed return current of the current drive  
25   circuit is supplied as drive current IOOUT to organic EL element Z1, whereby organic EL element Z1 is illuminated; and when switch means SW1 is turned OFF, drive current IOOUT becomes 0 and organic EL element Z1 is extinguished.

A similar configuration that employs a bipolar transistor is disclosed in FIG. 7 of Japanese Patent Laid-Open Publication No. 2001-042827.

However, the current drive circuit of the example of the prior art that is shown in FIG. 1 is a configuration in which switch means SW1 is connected  
5 between output terminal O1 and the drain terminal of p-channel MOS transistor M11, which is the output terminal of a current mirror circuit. As a result, when switch means SW1 is in the OFF state, the voltage between node A and node B of switch means SW1 is substantially the voltage difference between voltage VDD on the high level power supply VDD and ground, i.e., the low level power  
10 supply. In other words, the voltage difference is at an extremely high level that approaches voltage VDD, and the problem therefore arises that a large surge current is generated such as shown in FIG. 2 when switch means SW1 changes from the OFF state to the ON state. As an additional problem, the use of the basic current mirror circuit in the current drive circuit of the example of the  
15 prior art shown in FIG. 1 prevents the acquisition of a highly accurate return current.

#### Summary of the Invention:

The present invention was realized in view of the above-described  
20 problems and has as an object the provision of a current drive circuit that is capable of both obtaining a highly accurate drive current and suppressing the occurrence of a surge current, and further, to provide a display that is provided with such a current drive circuit.

The current drive circuit of the present invention is provided with: a  
25 current mirror circuit; a current source for applying reference current input to the current mirror circuit; a switch means to which the output current of the current mirror circuit is applied; and a cascode circuit for supplying the output current of

the switch means as a drive current.

In addition, the current drive circuit of the present invention is provided with a bias generator that includes: a first transistor in which the gate terminal and drain terminal are connected together; a second transistor in which the source terminal is connected to the drain terminal of the first transistor and in which the gate terminal and drain terminal are connected together; and a current supply that causes a reference current to flow to the second transistor; and a current output unit that includes: a third transistor in which the gate terminal is connected to the gate terminal of the first transistor; a fourth transistor in which the gate terminal is connected to the gate terminal of the second transistor; and a switch means that is provided between the drain terminal of the third transistor and the source terminal of the fourth transistor. In addition, a plurality of current output units, and a plurality of terminals that are connected to each of the drain terminals of the fourth transistors of the plurality of current output units may also be provided.

Each of the plurality of current output units may supply as output a current that has been weighted.

A plurality of the current drive circuits of the present invention and a terminal that is connected to the drain terminals of each of the fourth transistors of the plurality of current drive circuits may also be provided.

Each of the plurality of current drive circuits may supply as output a current that has been weighted.

The switch means may be turned ON and OFF by a control signal.

The control signals may be graduation data signals of a display.

The switch means may be a MOS transistor.

The switch means may be a switch group that includes a plurality of switch means, and the switch group may decode the graduation data signals of

the display.

A switch means that is connected to the source terminal of the third transistor may also be provided.

5 A switch means may also provided that is connected to the source terminal of the first transistor and that is always in the ON state.

The display of the present invention is provided with: organic EL elements that are arranged in a matrix; current drive circuits and scan circuits for causing drive currents to flow to the organic EL elements; and signal processing circuits for receiving image data signals as input, supplying  
10 graduation data signals as output to the current drive circuits, and supplying scan control signals as output to the scan circuits; and is provided with the above-described current drive circuit as a current drive circuit.

Accordingly, the present invention can realize a current drive circuit that is capable of obtaining a highly accurate drive current, and further, of  
15 suppressing the occurrence of a surge current, and that can realize a display that is provided with such current drive circuits.

The above and other objects, features, and advantages of the present invention will become apparent from the following description with reference to the accompanying drawings, which illustrate examples of the present invention.

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#### Brief Description of the Drawings:

FIG. 1 is a circuit diagram of a current drive circuit of the prior art;

FIG. 2 is an explanatory view of the operation of the current drive circuit of the prior art;

25 FIG. 3 is a circuit diagram of the current drive circuit of the first embodiment of the present invention;

FIG. 4 is an explanatory view of the operation of the current drive circuit

of the first embodiment of the present invention;

FIG. 5 is a circuit diagram of the current drive circuit of the second embodiment;

FIG. 6 is a circuit diagram of the current drive circuit of the third  
5 embodiment of the present invention;

FIG. 7 is a circuit diagram of the display of the fourth embodiment of the present invention;

FIG. 8 is a circuit diagram of the current drive circuit of the fifth embodiment of the present invention;

10 FIG. 9 is a circuit diagram of the current drive circuit of the sixth embodiment of the present invention;

FIG. 10 is a detailed circuit diagram of FIG. 9;

FIG. 11 is an explanatory view of the decoding operation of FIG. 10;  
and

15 FIG. 12 is a circuit diagram of the current drive circuit of the seventh embodiment of the present invention.

#### Detailed Description of the Preferred Embodiments:

Embodiments of the present invention are next described with  
20 reference to the accompanying drawings. First, referring to FIG. 3, the configuration of the current drive circuit of the first embodiment of the present invention is described. FIG. 3 is a circuit diagram of the current drive circuit of the first embodiment of the present invention. As shown in FIG. 3, the current drive circuit of the first embodiment of the present invention is provided with  
25 bias generator 10 and current output unit 11.

Bias generator 10 is provided with: p-channel MOS transistor M01, p-channel MOS transistor M02, and reference current source I1. The source

terminal of p-channel MOS transistor M01 is connected to high level power supply VDD, and the gate terminal of p-channel MOS transistor m01 and the drain terminal of p-channel MOS transistor m01 are connected together. The source terminal of p-channel MOS transistor M02 is connected to the drain terminal of p-channel MOS transistor M01, and the gate terminal of p-channel MOS transistor M02 and the drain terminal of p-channel MOS transistor M02 are connected together. Reference current source I1 is connected between the drain terminal of p-channel MOS transistor M02 and the ground, which serves as the low level power supply, and supplies constant current IREF to p-channel MOS transistor M02.

Current output unit 11 is provided with: p-channel MOS transistor M11, switch means SW1, p-channel MOS transistor M12, and output terminal O1. The source terminal of p-channel MOS transistor M11 is connected to the high level power supply VDD, and the gate terminal of p-channel MOS transistor M11 is connected to the gate terminal of p-channel MOS transistor M01. The gate terminal of p-channel MOS transistor M12 is connected to the gate terminal of p-channel MOS transistor M02, and the drain terminal of p-channel MOS transistor M12 is connected to output terminal O1. Switch means SW1 is provided between the drain terminal of p-channel MOS transistor M11 and the source terminal of p-channel MOS transistor M12. In other words, node A, which is one end of the ON/OFF path of switch means SW1, is connected to the drain terminal of p-channel MOS transistor M11, and node B, which is the other end of the ON/OFF path of switch means SW1, is connected to the source terminal of p-channel MOS transistor M12. Switch means SW1 is consisted of, for example, a p-channel MOS transistor, the source-drain path of this p-channel MOS transistor being the ON/OFF path of switch means SW1 and one-bit graduation data signal D1 being applied to the gate terminal of this

p-channel MOS transistor. Switch means SW1 is turned ON and OFF by graduation data signal D1, which is the ON/OFF control signal.

Organic EL element Z1 is then connected as load between output terminal O1 and ground.

5           Following explanation regards the operation. P-channel MOS transistor M01 and p-channel MOS transistor M11 operate as a current mirror circuit, p-channel MOS transistor M02 and p-channel MOS transistor M12 operate as a cascode circuit, and reference current source I1 operates by applying constant current IREF as input to p-channel MOS transistor M01 of the current mirror  
10   circuit by way of p-channel MOS transistor M02 of the cascode circuit. In this example, the channel length and channel width of p-channel MOS transistor M01 and p-channel MOS transistor M11 are identical, and the channel length and channel width of p-channel MOS transistor M02 and p-channel MOS  
15   transistor M12 are identical, but the channel length and channel width ratio of p-channel MOS transistor M01 and p-channel MOS transistor M11 may be altered to change the mirror ratio. Further, although the channel length and channel width of p-channel MOS transistor M01 and p-channel MOS transistor M02 are identical in this example, the channel length and channel width for the  
20   two p-channel MOS transistors M01 and M02 need not be identical. When constant current IREF is applied as input to p-channel MOS transistor M01 of the current mirror circuit, a current that is in units of constant current IREF is returned from p-channel MOS transistor M11 of the current mirror circuit and applied as input to switch means SW1. When graduation data signal D1  
25   becomes logic L level and switch means SW1 turns ON, the output current of p-channel MOS transistor M11 of the current mirror circuit is supplied from switch means SW1 and applied as input to p-channel MOS transistor M12 of the cascode circuit, and p-channel MOS transistor M12 of the cascode circuit

supplies the output current of switch means SW1 to output terminal O1 as drive current IOUT to illuminate organic EL element Z1. When graduation data signal D1 becomes logic H level and switch means SW1 is turned OFF, the output current of p-channel MOS transistor M11 of the current mirror circuit is cut off by switch means SW1, drive current IOUT that p-channel MOS transistor M12 of the cascode circuit supplies to output terminal O1 becomes 0, and organic EL element Z1 is extinguished.

Following explanation regards the voltage difference between node A and node B of switch means SW1 when switch means SW1 is in the OFF state.

Constant current IREF flows from reference current source I1 to both p-channel MOS transistor M01 and p-channel MOS transistor M02, p-channel MOS transistor M01 and p-channel MOS transistor M02 both operate in a saturated region, and the relations shown by following equations 1 and 2 can therefore be obtained if  $\beta = \mu \cdot COX$ . Here,  $\mu$  is the carrier mobility, COX is the gate oxide film capacitance,  $\lambda$  is the channel modulation effect coefficient, and L and W are the channel length and channel width of p-channel MOS transistor M01 and p-channel MOS transistor M02. Further, VTH1 represents the absolute value of the threshold voltage of p-channel MOS transistor M01, VGS1 is the absolute value of the voltage across the gate and source of p-channel MOS transistor M01, VDS1 is the absolute value of the voltage across the drain and source of p-channel MOS transistor M01, VTH2 is the absolute value of the threshold voltage of p-channel MOS transistor M02, VGS2 is the absolute value of the voltage across the gate and source of p-channel MOS transistor M02, and VDS2 is the absolute value of the voltage across the drain and source of p-channel MOS transistor M02. In the following equations,  $\cdot$  indicates multiplication,  $/$  indicates division,  $a^b$  indicates the bth power of a, and  $\sqrt{a}$  indicates the square root of a.



Equation 1:

$$I_{REF} = (1/2) \cdot \beta \cdot (W/L) \cdot (V_{GS1} - V_{TH1})^2 \cdot (1 + \lambda \cdot V_{DS1})$$

(Where  $V_{GS1} = V_{DS1}$ )

Equation 2:

5 
$$I_{REF} = (1/2) \cdot \beta \cdot (W/L) \cdot (V_{GS2} - V_{TH2})^2 \cdot (1 + \lambda \cdot V_{DS2})$$

(Where  $V_{GS2} = V_{DS2}$ )

The value of channel modulation effect coefficient  $\lambda$  is extremely small, and if this value is ignored in the interest of simplifying the explanation, equation 1 and equation 2 can be modified and the voltage across the gate-source of p-channel MOS transistor M01 and p-channel MOS transistor M02 can be represented as shown in the following equation 3 and equation 4.

Equation 3:

$$V_{GS1} = V_{TH1} + \sqrt{(2I_{REF} / \beta) \cdot (L/W)}$$

Equation 4:

15 
$$V_{GS2} = V_{TH2} + \sqrt{(2I_{REF} / \beta) \cdot (L/W)}$$

If the voltage of node A when switch means SW1 is in the OFF state is  $V_A$  and the voltage of node B when switch means SW1 is in the OFF state is  $V_B$ , then voltage  $V_A$  is substantially equal to the voltage  $V_{DD}$  of high level power supply  $V_{DD}$ , and the threshold voltage of p-channel MOS transistor M12 is equal to threshold voltage  $V_{TH2}$  of p-channel MOS transistor M02, whereby threshold voltage  $V_B$  becomes a voltage that is higher than the gate voltage of p-channel MOS transistor M02, i.e.,  $(V_{DD} - V_{GS1} - V_{GS2})$ , and lower than a voltage that is higher by  $V_{TH2}$  than the gate voltage of p-channel MOS transistor M02, i.e.,  $(V_{DD} - V_{GS1} - V_{GS2} + V_{TH2})$ . In other words, based on equation 3 and equation 4, the maximum of the voltage difference  $(V_A - V_B)$  of switch means SW1 can be approximated by equation 5 below.

Equation 5:

$$V_A - V_B = V_{TH1} + V_{TH2} + 2\sqrt{(2 I_{REF} / \beta) \cdot (L/W)}$$

Although the difference in voltage between node A and node B of switch means SW1 when switch means SW1 is in the OFF state is substantially voltage VDD in the current drive circuit of the prior-art example that was shown in FIG. 1, in the current drive circuit of the present embodiment, VTH1 and VTH2 are very small values as shown in Equation 5, and it can be seen that these values can be set far lower than voltage VDD despite the appropriate setting of IREF. As a result, the surge current of drive current IOUT that is generated when switch means SW1 changes from the OFF state to the ON state can be suppressed, as shown in FIG. 4.

The configuration can also be modified such that p-channel MOS transistor M01, p-channel MOS transistor M02, p-channel MOS transistor M11, and p-channel MOS transistor M12 are all modified to n-channel MOS transistors and the high and low power supply voltages reversed, and switch means SW1 can be changed to an n-channel MOS transistor.

As described in the foregoing explanation, the adoption of a cascode current mirror circuit configuration according to the current drive circuit of the first embodiment of the present invention allows a highly accurate drive current IOUT to be obtained. In addition, the adoption of a configuration in which switch means SW1 is provided between p-channel MOS transistor M11 and p-channel MOS transistor M12 obtains the effect of enabling a suppression of the surge current of drive current IOUT that occurs when switch means SW1 changes from the OFF state to the ON state. Finally, the suppression of the surge current and the reduction of the time required for drive current IOUT to stabilize obtains the effect of enabling high-speed operation.

The configuration of the current drive circuit of the second embodiment of the present invention is next described with reference to FIG. 5. FIG. 5 is a

circuit diagram of the current drive circuit of the second embodiment of the present invention. The only point of difference between the configuration of the current drive circuit of the second embodiment of the present invention shown in FIG. 5 and the configuration of the current drive circuit of the first embodiment of the present invention shown in FIG. 3 is the modification of providing a plurality of current output units to enable application to organic EL elements in matrix form in a display device, the other components being identical. Components that are the same in the configuration shown in FIG. 5 and the configuration shown in FIG. 3 are therefore identified by the same reference numerals, and redundant explanation of these identical elements is here omitted.

As shown in FIG. 5, the current drive circuit of the second embodiment of the present invention is provided with: bias generator 10; and  $n$  ( $n$  being a natural number equal to or greater than 2) current output units, from current output unit 11 and current output unit 12 up to current output unit 1 $n$ .

Current output unit 12 is provided with: p-channel MOS transistor M21; switch means SW2; p-channel MOS transistor M22; and output terminal O2. The source terminal of p-channel MOS transistor M21 is connected to high level power supply VDD, and the gate terminal of p-channel MOS transistor M21 is connected to the gate terminal of p-channel MOS transistor M01. The gate terminal of p-channel MOS transistor M22 is connected to the gate terminal of p-channel MOS transistor M02, and the drain terminal of p-channel MOS transistor M22 is connected to output terminal O2. Switch means SW2 is provided between the drain terminal of p-channel MOS transistor M21 and the source terminal of p-channel MOS transistor M22. Switch means SW2 is consisted of, for example, a p-channel MOS transistor, the source-drain path of this p-channel MOS transistor serving as the ON/OFF path of switch means

SW2, and the gate terminal of the p-channel MOS transistor being supplied with one-bit graduation data signal D2. Switch means SW2 is turned ON and OFF by graduation data signal D2, which is the ON/OFF control signal.

5       Organic EL element Z2 is connected as load between output terminal O2 and ground, organic EL element Z2 being illuminated when graduation data signal D2 becomes logic L level and switch means SW2 turns ON, and organic EL element Z2 being extinguished when graduation data signal D2 becomes the logic H level and switch means SW2 turns OFF.

10       Current output unit 1n is otherwise similarly provided with: p-channel MOS transistor Mn1, switch means SWn, p-channel MOS transistor Mn2, and output terminal On. The source terminal of p-channel MOS transistor Mn1 is connected to high level power supply VDD, and the gate terminal of p-channel MOS transistor Mn1 is connected to the gate terminal of p-channel MOS transistor M01. The gate terminal of p-channel MOS transistor Mn 2 is  
15       connected to the gate terminal of p-channel MOS transistor M02, and the drain terminal of p-channel MOS transistor Mn2 is connected to output terminal On. Switch means SWn is provided between the drain terminal of p-channel MOS transistor Mn1 and the source terminal of p-channel MOS transistor Mn2. Switch means SWn is consisted of, for example, a p-channel MOS transistor,  
20       the source-drain path of this p-channel MOS transistor serving as the ON/OFF path of switch means SWn, and one-bit graduation data signal Dn being applied to the gate terminal of this p-channel MOS transistor. Switch means SWn is turned ON and OFF by graduation data signal Dn, which is the ON/OFF control signal.

25       Organic EL element Zn is then connected between output terminal On and ground as load, organic EL element Zn being illuminated when graduation data signal Dn becomes logic L level and switch means SWn turns ON, and

organic EL element Zn being extinguished when graduation data signal Dn becomes logic H level and switch means SWn is turned OFF.

As described in the preceding explanation, the current drive circuit of the second embodiment of the present invention can obtain the effect of enabling the simultaneous and individual drive of n organic EL elements from organic EL element Z1 and organic EL element Z2 to organic EL element Zn by means of a configuration in which the n current output units, from current output unit 11 and current output unit 12 to current output unit 1n, are caused to generate the same drive current from reference current source I1 of bias generator 10, and in which n bits of graduation data signals, from graduation data signal D1 and graduation data signal D2 to graduation data signal Dn, exercise ON/OFF control over switch means, from switch means SW1 and switch means SW2 to switch means SWn.

Following explanation regards the configuration of the current drive circuit of the third embodiment of the present invention with reference to FIG. 6. FIG. 6 is a circuit diagram of the current drive circuit of the third embodiment of the present invention. The only point of difference between the configuration of the current drive circuit of the third embodiment of the present invention that is shown in FIG. 6 and the configuration of the current drive circuit of the second embodiment of the present invention that is shown in FIG. 5 is the modification whereby the output terminals of each of the n current output units, from current output unit 11 and current output unit 12 to current output unit 1n, are connected to a single output terminal O1. The components are otherwise identical, and the same reference numerals are therefore applied to identical components in the configuration shown in FIG. 6 and the configuration shown in FIG. 5, and redundant explanation regarding these components is here omitted.

As shown in FIG. 6, the drain terminals of each of n p-channel MOS

transistors from p-channel MOS transistor M12 and p-channel MOS transistor M22 to p-channel MOS transistor Mn2 are connected in common to output terminal O1, and organic EL element Z1 is connected as load between output terminal O1 and ground. Graduation control can thus be exercised over the drive current of organic EL element Z1 by using the n current output units from current output unit 11 and current output unit 12 to current output unit 1n.

When the output currents of each of the n current output units, from current output unit 11 and current output unit 12 to current output unit 1n, are equal, a drive current can be obtained that enables n graduation variations by changing the number of switch means among the n switch means, from switch means SW1 and switch means SW2 to switch means SWn, that are turned ON by the n bits of graduation data signals, from graduation data signal D1 and graduation data signals D2 to graduation data signal Dn. In addition, binary weighting of the mirror ratio of the return currents of the n current output units, from current output unit 11 and current output unit 12 to current output unit 1n, enables the representation of the output current of each of the n current output units, from current output unit 11 and current output unit 12 to current output unit 1n, by:

$$2^{(i-1)} \cdot I_{REF}$$

where i is a natural number equal to or less than n. A drive current can thus be obtained that is capable of  $2^n$  graduation variations.

As described in the foregoing explanation, the current drive circuit of the third embodiment of the present invention has the effect of obtaining a drive current that allows n graduation variations and a drive current that allows  $2^n$  graduation variations.

Following explanation regards the configuration of the display of the fourth embodiment of the present invention with reference to FIG. 7. FIG. 7 is a

circuit diagram of the display of the fourth embodiment of the present invention.

As shown in FIG. 7, the display of the fourth embodiment of the present invention is provided with: signal processing circuit 60, current drive circuit 61, scan circuit 62, and organic EL elements 63 that are arranged in matrix form in m (where m is a natural number equal to or greater than 2) rows and n (where n is a natural number equal to or greater than 2) columns. Signal processing circuit 60, upon input of a one-screen portion of image data signals 64,

sequentially applies one-row portions of gradation data signals 65 to current drive circuit 61, and with each output of a one-row portion of gradation data signals 65, applies scan control signal 66 to scan circuit 62. Each of the n bits of gradation data signals 65 has a one-to-one correspondence to the n organic EL elements 63 in one row, and the illumination or darkening of corresponding organic EL elements 63 is designated by the logic level of each bit. Current drive circuit 61 is provided with n output terminals, from output terminal O1 to

output terminal On, that have a one-to-one correspondence to each bit of gradation data signal 65, and a drive current flows from an output terminal to the positive electrode terminal of organic EL element 63 when the corresponding bit is logic L level, and drive current does not flow from an output terminal when the corresponding bit is logic H level. The n negative electrode

terminals of one-row portions of organic EL elements 63 are connected in common to corresponding output terminals of scan circuit 62, from output terminal C1 to output terminal Cm; and ground level output is sequentially supplied as the low level power supply to one output terminal, from output terminal C1 to output terminal Cm, in accordance with scan control signals 66.

Then, of the m rows and n columns of organic EL elements 63, those organic EL elements in which the drive current flows to the positive electrode terminals and the ground level is applied to the negative electrode terminals are

illuminated, and the remaining organic EL elements 63 are extinguished.

Although a configuration is shown in the third embodiment in which a drive current that has been subjected to graduation control is supplied to a single organic EL element, the current drive circuit of the third embodiment may  
5 be provided for each of output terminals from output terminal O2 to output terminal On for application to the display of the fourth embodiment of the present invention.

The current drive circuit of the third embodiment of the present invention that was shown in FIG. 6 is applied in current drive circuit 61, and  
10 graduation data signals 65 become the n bits of graduation data signals, from graduation data signal D1 and graduation data signal D2 to graduation data signal Dn, that are shown in FIG. 6.

As described in the foregoing explanation, through the provision of the current drive circuits of the third embodiment of the present invention that  
15 supply a drive current in which the surge current is suppressed with both high accuracy and high speed, the display of the fourth embodiment of the present invention obtains the effect of enabling the realization of a display that is capable of high-speed display with high quality.

Following explanation regards the configuration of the current drive  
20 circuit of the fifth embodiment of the present invention with reference to FIG. 8. FIG. 8 is a circuit diagram of the current drive circuit of the fifth embodiment of the present invention. The current drive circuit of the fifth embodiment of the present invention that is shown in FIG. 8 is provided with: n (where n is a natural number equal to or greater than 2) current drive circuits of the first  
25 embodiment of the present invention that was shown in FIG. 3, the output terminals of each of the n current drive circuits, from current drive circuit 21 and current drive circuit 22 to current drive circuit 2n, being connected to a single



output terminal O1. Components in the configuration shown in FIG. 8 that are identical to components in the configuration shown in FIG. 3 are given the same reference numerals and redundant explanation is here omitted.

The configuration of the  $n$  current drive circuits, from current drive circuit 21 and current drive circuit 22 to current drive circuit  $2n$ , is identical. In other words, the p-channel MOS transistors, from p-channel MOS transistor M01 and p-channel MOS transistor M03 up to p-channel MOS transistor M02 $n$  – 1, are identical; the p-channel MOS transistors from p-channel MOS transistor M11 and p-channel MOS transistor M21 up to p-channel MOS transistor M $n$ 1 are identical; the p-channel MOS transistors from p-channel MOS transistor M02 and p-channel MOS transistor M04 up to p-channel MOS transistor M02 $n$  are identical; the p-channel MOS transistors from p-channel MOS transistor M12 and p-channel MOS transistor M22 up to p-channel MOS transistor M $n$ 2 are identical; the reference current sources from reference current source I1 and reference current source I2 up to reference current source I $n$  are identical; and the switch means from switch means SW1 and switch means SW2 up to switch means SW $n$  are identical.

As shown in FIG. 8, each of the drain terminals of the  $n$  p-channel MOS transistors, from p-channel MOS transistor M12 and p-channel MOS transistor M22 up to p-channel MOS transistor M $n$ 2, are connected in common to output terminal O1; and organic EL element Z1 is connected as load between output terminal O1 and ground. The  $n$  current drive circuits, from current drive circuit 21 and current drive circuit 22 up to current drive circuit  $2n$ , can be used to realize graduation control of the drive current of organic EL element Z1.

Although a configuration has been shown in the present embodiment in which drive currents that have undergone graduation control are supplied in common to a single organic EL element; the current drive circuits of the present

embodiment should be provided for each of output terminals from output terminal O2 to output terminal On for application to the display of the third embodiment of the present invention.

When the output currents of each of the n current drive circuits, from current drive circuit 21 and current drive circuit 22 up to current drive circuit 2n, are equal, a drive current can be obtained that enables n graduation variations by changing the number of switch means among the n switch means, from switch means SW1 and switch means SW2 to switch means SWn, that are turned ON by the n bits of graduation data signals from graduation data signal D1 and graduation data signals D2 to graduation data signal Dn. In addition, binary weighting of the constant-current value of the n current drive circuits, from current drive circuit 21 and current drive circuit 22 up to current drive circuit 2n, enables the representation of the weighted output current of each of the n current drive circuits, from current drive circuit 21 and current drive circuit 22 up to current drive circuit 2n, by:

$$2^{(i-1)} \cdot I_{REF}$$

where i is a natural number equal to or less than n. A drive current can thus be obtained that is capable of  $2^n$  graduation variations.

As described in the foregoing explanation, the current drive circuit of the fifth embodiment of the present invention has the effect of obtaining a drive current that allows n graduation variations and a drive current that allows  $2^n$  graduation variations.

Following explanation regards the configuration of the current drive circuit of the sixth embodiment of the present invention with reference to FIGs. 9, 10, and 11. FIG. 9 is a circuit diagram of the current drive circuit of the sixth embodiment of the present invention, FIG. 10 is a detailed view of the circuit diagram of FIG. 9, and FIG. 11 is an explanatory view of the decoding operation

of FIG. 10. The only points of difference between the configuration of the current drive circuit of the sixth embodiment of the present invention that is shown in FIG. 9 and the configuration of the current drive circuit of the fourth embodiment of the present invention that is shown in FIG. 7 are the

5 modification of the  $n$  switch means, from switch means SW1 and switch means SW2 up to switch means SW $n$ , to  $n$  switch groups, from switch group SG1 and switch group SG2 up to switch group SG $n$ , that each include a plurality of switch means; and the modification of the  $n$  current output units, from current output unit 11 and current output unit 12 to current output unit 1 $n$ , to  $n$  current  
10 output units, from current output unit 31 and current output unit 32 to current output unit 3 $n$ . The components are otherwise identical, and components shown in FIG. 9 that are identical to components shown in FIG. 7 are therefore identified by the same reference numerals and redundant explanation is here omitted.

15 The current drive circuit of the fourth embodiment of the present invention that is shown in FIG. 7 is provided with only one switch means for each of the  $n$  current output units, from current output unit 11 and current output unit 12 up to current output unit 1 $n$ . As a consequence, in a case in which the output currents of each of the  $n$  current output units, from current output unit 11  
20 and current output unit 12 up to current output unit 1 $n$ , are equal and  $n$  graduation control is to be implemented, and when the graduation data signals, from graduation data signal D1 and graduation data signal D2 up to graduation data signal D $n$ , are binary code of  $n$  bits, an external decoder is required for placing the graduation data signals, from graduation data signal D1 and  
25 graduation data signal D2 up to graduation data signal D $n$ , in correspondence with the switch means, from switch means SW1 and switch means SW2 up to switch means SW $n$ . To eliminate the need for this decoder, the present

embodiment is provided with switch groups, from switch group SG1 and switch group SG2 up to switch group SGn, for decoding the graduation data signals, from graduation data signal D1 and graduation data signal D2 up to graduation data signal Dn.

5           A more detailed explanation is presented using FIG. 10 and FIG. 11. As the details of a specific example of the configuration of the switch groups of FIG. 9, from switch group SG1 and switch group SG2 up to switch group SGn, FIG. 10 shows a configuration in which seven current output units are controlled by three bits of graduation data signals, graduation data signal D1, graduation data  
10   signal D2, and graduation data signal D3. FIG. 11 shows the relation between the graduation data signals, switch means that are ON, and drive current IOUT.

Switch group SG1 is provided with switch means SW11, switch means SW12, and switch means SW13 that are parallel-connected, both ends of switch means SW11 being connected between the drain terminal of p-channel  
15   MOS transistor M11 and the source terminal of p-channel MOS transistor M12. Switch group SG2 is provided with: switch means SW21 that is always in the ON state, and switch means SW22 and switch means SW23 that are parallel connected to each other and serially connected to switch means SW21; one end of switch means SW21 and one end of switch means SW22 being  
20   connected between the drain terminal of p-channel MOS transistor M21 and the source terminal of p-channel MOS transistor M22.

Switch group SG3 is provided with switch means SW33, and switch means SW31 and switch means SW32 that are parallel connected to switch means SW33, these two switch means SW31 and switch means SW32 being  
25   serially connected, and both ends of switch means SW33 being connected between the drain terminal of p-channel MOS transistor M31 and the source terminal of p-channel MOS transistor M32.

Switch group SG4 is provided with serially connected switch means SW41 that is always in the ON state, switch means SW42 that is always in the ON state, and switch means SW43; one end of switch means SW41 and one end of switch means SW43 being connected between the drain terminal of p-channel MOS transistor M41 and the source terminal of p-channel MOS transistor M42.

Switch group SG5 is provided with switch means SW53, and switch means SW51 and switch means SW52 that are parallel connected to each other and serially connected to switch means SW53; one end of switch means SW51 and one end of switch means SW53 being connected between the drain terminal of p-channel MOS transistor M51 and the source terminal of p-channel MOS transistor M52.

Switch group SG6 is provided with serially connected switch means SW61 that is always in the ON state, switch means SW62, and switch means SW63; one end of switch means SW61 and one end of switch means SW63 being connected between the drain terminal of p-channel MOS transistor M61 and the source terminal of p-channel MOS transistor M62.

Switch group SG7 is provided with serially connected switch means SW71, switch means SW72, and switch means SW73; one end of switch means SW71 and one end of switch means SW73 being connected between the drain terminal of p-channel MOS transistor M71 and the source terminal of p-channel MOS transistor M72. In the above-described configuration, switch means that are always in the ON state can be omitted.

Switch means SW11, switch means SW31, switch means SW51, and switch means SW71 are subjected to ON/OFF control by graduation data signal D1, which is the LSB of three bits; switch means SW12, switch means SW22, switch means SW32, switch means SW52, switch means SW62, and switch

means SW72 are subjected to ON/OFF control by graduation data signal D2; and switch means SW13, switch means SW23, switch means SW33, switch means SW43, switch means SW53, switch means SW63, and switch means SW73 are subjected to ON/OFF control by graduation data signal D3, which is the MSB of three bits.

As shown in FIG. 11, when graduation data signal D1, graduation data signal D2, and graduation data signal D3, which are a three-bit binary code, are changed from (000) to (111) by means of the above-described configuration, drive current IOUT, which takes the constant-current IREF of reference current source I1 as a variable step, can be obtained from 0 to 7 IREF. For the sake of convenience, a case was shown in FIG. 11 in which the switch means was ON when the graduation data signal was logic 1, but logic 1 corresponds to logic level L when the switch means is consisted of a p-channel MOS transistor. In addition, although a configuration was shown in FIG. 10 in which seven current output units are controlled by three bits, i.e., graduation data signal D1, graduation data signal D2, and graduation data signal D3, it is extremely easy to provide n switch groups, from switch group SG1 and switch group SG2 up to switch group SGn, that each include a plurality of switch means, and to expand to n current output units, from current output unit 31 and current output unit 32 to current output unit 3n.

It should be clear that the configuration of switch groups from switch group SG1 and switch group SG2 up to switch group SGn can be applied to the configuration of current drive circuit of the fifth embodiment of the present invention that is shown in FIG. 8.

As described in the foregoing explanation, by adopting a configuration that is provided with switch groups from switch group SG1 and switch group SG2 up to switch group SGn for carrying out a decoding operation, the current

drive circuit of the sixth embodiment of the present invention obtains the effect of enabling n-graduation control by direct linking even when the graduation data signals, from graduation data signal D1 and graduation data signal D2 up to graduation data signal Dn, are binary codes of n bits.

5           Following explanation regards the configuration of the current drive circuit of the seventh embodiment of the present invention with reference to FIG. 12. FIG. 12 is a circuit diagram of the current drive circuit of the seventh embodiment of the present invention. As the only point of difference between the configuration of the current drive circuit of the seventh embodiment of the present invention shown in FIG. 12 and the configuration of the current drive  
10           circuit of the sixth embodiment of the present invention shown in FIG. 9, in each switch group of the n switch groups from switch group SG1 and switch group SG2 up to switch group SGn that each include a plurality of switch means, one portion of the switch means that are included in switch groups and that are  
15           connected together in a series is shifted to the source side of a p-channel MOS transistor of the current mirror circuit to which its switch group is connected. The two configurations are otherwise identical, and components that are identical in the configuration shown in FIG. 12 and in the configuration shown in FIG. 9 are therefore identified by the same reference numerals and redundant explanation  
20           is here omitted.

          Bias generator 40 is a configuration in which switch means SW00 is connected between high level power supply VDD and the source terminal of p-channel MOS transistor M01 of bias generator 10 that is shown in FIG. 9; current output unit 51 is a configuration in which switch means SW01 is  
25           connected between high level power supply VDD and the source terminal of p-channel MOS transistor M11 of current output unit 31 that is shown in FIG. 9; current output unit 52 is a configuration in which switch means SW02 is

connected between high level power supply VDD and the source terminal of p-channel MOS transistor M21 of current output unit 32 shown in FIG. 9; and current output unit 5n is a configuration in which switch means SW0n is connected between high level power supply VDD and the source terminal of p-channel MOS transistor Mn1 of current output unit 3n shown in FIG. 9. Switch means SW00 that is always ON in bias generator 40 is provided for connecting the same ON resistance (the resistance across the source and drain of a p-channel MOS transistor) as the ON resistance (the resistance across the source and drain of the p-channel MOS transistor) of switch means from switch means SW01 and switch means SW02 up to switch means SW0n in order to realize highly accurate current mirror operation.

Because a portion of the switch means has been removed, the n switch groups from switch group SG1 and switch group SG2 up to switch group SGn are modified to n switch groups from switch group SG01 and switch group SG02 up to switch group SG0n.

According to the configuration shown in FIG. 10,  $n = 7$ , whereby, for example, switch means SW11, switch means SW12, and switch means SW13 that are connected together in parallel are switch means SW01; switch means SW21 that is always in the ON state is switch means SW02; and switch means SW71 is switch means SW07.

As described in the foregoing explanation, the current drive circuit of the seventh embodiment of the present invention obtains the same effect as the current drive circuit of the sixth embodiment of the present invention.

While preferred embodiments of the present invention have been described using specific terms, such description is for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.